Unit -5(mcq)

2.1 The features in which PDSP is superior to advanced microprocessors is———. (a) Low cost (b) Low power (c) Computational speed (d) Real time I/O capability

2.2 In modifi ed Harvard architecture for fetching the content of program and data memory, a separate bus is used for ——— memory and a single bus is used for ——— memory.

2.3 Number of memory accesses/clock /period that can be achieved using on chip DARAM of a P-DSP is ———. (a) 1 (b) 2 (c) 3 (d) 4

2.4 VLIW architecture differs from conventional P-DSP in which of the following aspects: (a) Instruction cache (b) Number of functional units (c) Use pipelining (d) A single word fetched from memory has a number of instructions

2.5 A P-DSP has four pipeline stages and uses four phase clock. The number of clock cycles required for executing a program with 25 instruction is ———. (a) 29 (b) 28 (c) 25 (d) 26

2.6 The number of instruction cycles required for executing a program in a microprocessor with no pipelining is ———. (a) 1 (b) 2 (c) 3 (d) 4

2.7 The addressing mode that is convenient for FFT computation is———. (a) Indirect addressing (b) Circular mode (c) Bit reversed addressing (d) Memory mapped

The addressing mode that is convenient for FFT computation is

(a)bit reversed addressing

2.8 The addressing that permits the content in internal register of the CPU & I/O to be accessed as memory location is———. (a) Indirect addressing (b) Circular mode (c) Bit reversed addressing (d) Memory mapped

2.9 The serial port that permits the data from a number of I/O devices to be sent using a single serial port is called———. (a) Comm port (b) Host port (c) Time division multiplexing (d) Bit I/O port

2.10 Which of the following characteristics are true for a RISC processor? (a) Smaller control unit (b) Small instruction set (c) Short program length (d) Less traffi c between CPU & memory

3.1 The 320C5X DSPs are said to have advanced Harvard architecture because

(a) they have separate memory bus structures for program and data (b) they have instructions that enable data transfer between the program and data memory area (c) they have same memory bus structures for program and data (d) the contents of program memory cannot into the data memory or vice versa

3.2 The central ALU of C5X DSP processors have ——— bit ALU and one of the operands for the ALU operation comes from ———. (a) 32,ACC (b) 16,ACC (c) 32,ACCB (d) 16,ACCB

3.3 The result of operations performed in central ALU are stored in ———. (a) ACC (b) ACCB (c) TREG0 (d) PREG

3.4 The ALU register whose either higher order word or lower order word can be loaded from memory is.

(a) ACC (b) ACCB (c) TREG0 (d) PREG

3.5 The ——— bit register used for temporary storage of accumulator is ———. (a) 32, PREG (b) 32, ACCB (c) 16, TREG0, (d) 32, ACC

3.6 The ——— permits execution of logical operations on data without affecting the contents of ACC. (a) parallel logic unit (b) auxiliary ALU (c) central ALU

3.7 The hardware multiplier unit in the C5X processors perform multiplication of ——— times ——— bit represented in ——— complement form. (a) 16, 16, 1s (b) 8,8 1s (c) 16, 16, 2s (d) 8, 8, 2s

3.8 ——— holds the result of multiplication and is ——— bit wide. (a) PREG, 32 (b) PREG, 16 (c) TREG0, 16 (d) TREG0, 32

3.9 The register in which the multiplicand is stored before multiplication is performed is ——— and is ——— bit wide. (a) PREG, 32 (b) PREG, 16 (c) TREG0, 16 (d) TREG0, 32

3.10 ——— permits the contents of memory to be left shifted by 0-16 bits before they are either fed to ALU or stored from ALU to memory. (a) Scaling shifter (b) ALU (c) PLU (d) Auxiliary ALU

3.11 The register that specifi es the number of bits by which the scaling shifter should shift either the incoming data to one of the CPU registers or vice versa is ——— and is ——— bit wide. (a)TREG1,4 (b) TREG1, 5 (c) TREG2, 5 (d) TREG2, 4

3.12 When the incoming data to CPU is left shifted by the scaling shifter the LSBs are fi lled with ——— (a) 0 (b) 1 (c) LSB before shifting

3.13 The bit of status register ST1, which determines whether the MSBs of the bits left shifted by the scaling shifter is zero, are sign extended is ———. (a) SXM (b) TC (c) OV (d) OVM

3.14 In the hardware stack of C5X processors ——— bit numbers can be stored. (a) 16, 16 (b) 16, 8 (c) 8, 8 (d) 8, 16

3.15 The bit of status register 0 (ST0) that becomes 1 if overfl ow occurs from an ALU operation is ——— (a) SXM (b) OV (c) OVM (d) TC (e) C

3.16 The bit of ST0 that determines whether the ACC is replaced with either largest positive or negative number or left unmodifi ed is ———. (a) SXM (b) OV (c) OVM (d) TC (e) C

3.17 The bit of ST1 that is used for testing whether a particular memory is zero or not or for comparing one register against another register memory is ———. (a) SXM (b) OV (c) OVM (d) TC (e) C

3.18 The bit of ST1 that becomes 1 if either addition generates a carry or subtraction results in borrow is ———. (a) SXM (b) OV (c) OVM (d) TC (e) C

3.19 The status register bit that determines whether multiplier’s 32-bit product is left shifted by 0, 1, 4 or right shifted by 6 with sign extension before it is transferred/ added to the ACC is ———. (a) PM (b) CNF (c) HM (d) XF (e) INTM

3.20 The RAM confi guration control bit that indicates whether the on-chip reconfi gurable dual-access RAM is mapped to data space or program space is ———. (a) PM (b) CNF (c) HM (d) XF (e) INTM

3.21 The bit of status register that determines whether the processor halts the internal operation while acknowledging a hold or not is ———. (a) PM (b) CNF (c) HM (d) XF (e) INTM

3.22 The ——— bit of the status register indicates the status of the general purpose output pin. (a) PM (b) CNF (c) HM (d) XF (e) INTM

3.23 The pointers that are contained in the status register 0 are ———. (a) ARP (b) DP (c) ARB (d) IPTR (e) INTM

3.24 The pointers that are contained in the status register 1 are ———. (a) ARP (b) DP (c) ARB (d) IPTR (e) INTM

3.25 If ——— bit is set to 0, all unmasked interrupts are enabled. Otherwise all the maskable interrupts are disabled. (a) ARP (b) DP (c) ARB (d) IPTR (e) INTM

4.1 The data memory used with C5X processors is split into ——— pages each of ——— words long. (a) 512, 128 (b) 256, 256 (c) 128, 512 (d) 1024, 64

4.2 The register which holds the address of the current data memory page is ———. (a) DP (b) ARP (c) ARB

4.3 No. of words of program memory, data memory that can be addressed by C5X processors are ——, ——. (a) 64K,64K (b) 64K, 96K (c) 96K, 64K (d) 96K, 96K

4.4 The memory-mapped direct addressing mode is used to access data in page ———. (a) 1 (b) 0 (c) 511 (d) 512

4.5 The no. of registers which can be used for accessing data using indirect addressing mode is ———. (a) 16, 16 (b) 16, 8 (c) 8, 8 (d) 8, 16

4.6 The registers used for indirect addressing of memory are called ———. (a) auxiliary registers (ARs) (b) block move address register (BMAR) (c) TREGn

(d) index register (INDX)

4.7 In the indirect addressing mode, out of the eight ARs, the one which is currently used for accessing data is denoted by the register ———. (a) ARB (b) ARP (c) DP (d) BRCR

4.8 The register which is used for storing the contents of ARP temporarily is (a) ARB (b) DP (c) TREG1 (d) TREG2 (e) TREG3

4.9 When an operand for an instruction is accessed using the indirect addressing mode and the content of the AR used for accessing the data is to be left unaltered after the instruction is executed, the addressing mode is specifi ed by the symbol ———. (a) # (b) \* (c) \*– (d) \*+

4.10 When an operand for an instruction is accessed using the indirect addressing mode and the content of the auxiliary register used for accessing the data is to be decremented after the instruction is executed, the addressing mode is specifi ed by the symbol ———.(a) # (b) \* (c) \*– (d) \*+

4.11 The 16-bit register used with indirect addressing mode for testing whether an increment/decrement operation of an AR has exceeded a particular value or not is ———. (a) ARCR (b) ARP (c) ARB (d) INDX

4.12 The 16-bit register used for incrementing/ decrementing the ARn in steps larger than 1 is ———. (a) ARCR (b) ARP (c) ARB (d) INDX

4.13 The contents of ARs are decremented/incremented using ———. (a) central ALU (b) auxiliary ALU (c) PLU

4.14 When an operand for an instruction is accessed using the indirect addressing mode and after the data is fetched, the content of the AR used for accessing the data is to be decremented by the number in INDX register, the addressing mode is specifi ed by the symbol ———. (a) \*0+ (b) \*0– (c) \*BR0+ (d) \*BR0-

4.15 When an operand for an instruction is accessed using the indirect addressing mode and after the data is fetched, the content of the AR used for accessing the data is to be incremented by the number in INDX register with reverse carry propagation, the addressing mode is specifi ed by the symbol ———. (a) \*0+ (b) \*0– (c) \*BR0+ (d) \*BR0–

4.16 The AR ALU (ARAU) performs ——— arithmetic on ——— numbers. (a) unsigned, 16 (b) signed, 16 (c) signed, 32 (d) unsigned, 32

4.17 The symbol used to indicate the immediate address mode for the operand is ———. (a) $ (b) \* (c) # (d) \*-(e)\*+

4.18 In the dedicated register addressing mode, the register whose contents are used if an immediate operand is unspecifi ed is ———. (a) ARCR (b) BMAR (c) DBMR (d) ACCB

4.19 Before the instruction SBRK #5H is executed, the contents of ARP, AR3 and AR5 are 3H, 1058H and 1000H, respectively. After the execution of the instruction, the content of AR3 is ———. (a) 5H (b) 1053H (c) 1058H (d) 1000H

4.20 Assume that the contents of ACC, ARP, AR3 and locations 0045H, 40C5H are 1000H, 3, 40C5H and 2400,2300H, respectively, initially. When the instruction LAMM \* is executed, the content of ACC is ———. (a) 2400H (b) 2300H (c) 40C5H (d) 0003H

4.21 The mnemonic for the instruction used to move a word from data memory to program memory is ———.

(a) BLDD (b) BLDP (c) BLPD (d) TBLR (e) TBLW

4.21 The mnemonic for the instruction used to move a word from data memory to program memory and in which the program memory address is contained in ACC lower order word is ———. (a) BLDD (b) BLDP (c) BLPD (d) TBLR (e) TBLW

4.22 The mnemonic for the instruction which multiplies two 16-bit numbers represented in 2’s complement form is ———. (a) MPYA (b) MPY (c) MPYU (d) MPYS (e) MADD (f) MADS

4.23 The mnemonic for the instruction which loads zero into PREG is ———. (a) SQRA (b) SQRS (c) ZPR (d) ZAP

4.24 The mnemonic for the instruction which makes the program to branch unconditionally is ———. (a) B (b) BACC (c) BANZ (d) BCND

4.25 Using the RPT #k instruction, the maximum no. of times a single instruction can be repeatedly executed is ———. (a) 65535 (b) 255 (c) 256 (d) 65536

4.26 The mnemonic for the instruction which executes next k instructions repeatedly and which clears both ACC and PREG before starting the execution of the block of instructions is ———. (a) RPTB #k (b) RPTB #(k–1) (c) RPTZ #k (d) RPTZ #(k–l)

4.27 The IN instruction of C5X reads a ——— number from input port and stores it in ———. (a) 8, ACC (b) 8, memory (c) 16, ACC (d) 16, memory

4.28 The mnemonic for the instruction which forces the program being executed to wait until an unmasked interrupt or reset occurs is ———. (a) NOP (b) IDLE (c) IDLE2 (d) XC

4.29 The mnemonic for the instruction which executes the next n instructions if the condition specifi ed with the instruction is met else it executes NOPs for the next n instructions is ——— n conditions. (a) XC (b) RPT (c) RPTB (d) RPTZ

5.1 The program containing ——— instructions will ensure perfect overlapping of the operations in the four stages of the instruction pipeline of 5X. (a) single-word single-cycle (b) both single-word and double-word (c) delayed branch (d) delayed call

5.2 The number of clock cycles required for fl ushing out the pipeline in the case of execution of branch instruction B begin is ———. (a) 0 (b) 1 (c) 2 (d) 3

5.3 The number of clock cycles required for fl ushing out the pipeline in the case of execution of delayed branch instruction BD BEGIN is ———. (a) 0 (b) 1 (c) 2 (d) 3

5.4 The number of single-cycle instructions which can be executed after the delayed branch instruction of 5X before the execution begins the new branch address is ———. (a) 0 (b) 1 (c) 2 (d) 3

5.5 The number of double-cycle instructions which can be executed after the delayed branch instruction of 5X before the execution begins the new branch address is ———. (a) 0 (b) 1 (c) 2 (d) 3

5.6 Which of the following instructions does not require the instruction pipeline to be fl ushed out before executing additional instructions? (a) CC cond when cond true (b) CC cond when cond false (c) RETC cond when cond true (d) RETC cond when cond false

5.7 In which phase of the instruction pipeline, the AR is modifi ed when the instruction LACC \*+ is executed? (a) Fetch (b) Decode (c) Read (d) Execute

5.8 In which phase of the instruction pipeline, AR is modifi ed when the instruction LAR AR0 #1000h is executed? (a) Fetch (b) Decode (c) Read (d) Execute

5.9 In 5X programs using indirect addressing mode, to ensure proper operation the number of singleword instructions that should be inserted between the instruction which loads an AR and an instruction which fetches the operand using this AR is ———. (a) 1 (b) 2 (c) 3 (d) 4

5.10 An external memory used with 5X requires three clock cycles, the number of dummy operations carried out by the 5X CPU to avoid pipeline confl ict is ———. (a) 1 (b) 2 (c) 3 (d) 4

6.10 When the instruction BANZ loopl, AR1 is executed which of the following operations are performed? (a) branching occurs to loop 1 if the current AR is nonzero. (b) current AR content is decremented before branching (c) branching occurs if AR1 is non-zero (d) ARP made to point to AR1 after branching

6.11 The timer of C5X is an on-chip-counter and interrupt (TINT) is generated each time the counter reaches the state ———. (a) down, all l’s (b) down, all 0’s (c) up, all l’s (d) up, all 0’s

6.12 The signals used to connect the transmit pins of the serial port of C5X with the receiving device for data transmission are ———. (a) CLKX (b) DX (c) FSX (d) CLKR (e) RX (f) FSR

6.13 The signals used to connect the receive pins of the serial port of C5X with the transmitting device data reception are ———. (a) CLKX (b) DX (c) FSX (d) CLKR (e) RX (f) FSR

6.14 The registers of on-chip serial port of C5X which cannot be directly accessed by the CPU are (a) SPC (b) DXR (c) DRR (d) XSR (e) RSR 6.15 The registers of on-chip serial port of C5X which shifts the data serially in or out are (a) SPC (b) DXR (c) DRR (d) XSR (e) RSR

6.15 Writing the data into ——— of serial port of C5X generates the XINT. (a) SPC (b) DXR (c) DRR (d) XSR (e) RSR

6.16 Writing the data into ——— of serial port of C5X generates the RINT. (a) SPC (b) DXR (c) DRR (d) XSR (e) RSR 6.17 The signals which initiate the serial shifting of the data in the on-chip serial port at the beginning of every frame in burst mode and for the fi rst frame in the synchronous transfer mode for the shift registers used at the receive and transmit side respectively are ———. (a) CLKX (b) DX (c) FSX (d) CLKR (e) RX (f) FSR

6.18 In the AIC, the registers which are used to obtain the switched capacitor frequency of 288 kHz are (a) TX counter A, TX counter B (b) TX counter A, RX counter A (c) RX counter A, RX counter B (d) TX counter B, RX counter A

6.19 In the AIC, the registers which are used to obtain the required sampling frequency are ———. (a) TX counter A, TX counter B (b) TX counter A, RX counter A (c) RX counter A, RX counter B (d) TX counter B, RX counter B

6.20 To program the AIC, the secondary communication is initiated by choosing the d0, dl bits of the data transmitted through the DX pin in the primary communication mode as ———, ———. (a) 0, 0 (b) 1, 0 (c) 0, 1 (d) 1,1

6.21 256 samples of a sine wave of frequency 1000 Hz are stored in data memory organised as a circular buffer of size 256. The data is read one after another from this buffer and transmitted through the DX pin infi nitely. The frequency at the output of the AIC is ——— Hz. (a) 1000 (b) 500 (c) 2000 (d) 4000

6.22 256 samples of a sine wave of frequency 1000 Hz are stored in data memory organised as a circular buffer of size 256. The data is read one after another from this buffer and the alternate data is transmitted through the DX pin infi nitely. The frequency at the output of the AIC is ——— Hz. (a) 1000 (b) 500 (c) 2000 (d) 4000

10.1 No. of Auxiliary Register ALU(s) in 54X is ——— and number of data buses which can be used for reading data from data memory is ———. (a) 1, 1 (b) 1, 2 (c) 2, 1 (d) 2, 2

10.2 Which of the following are available in 54X but not in 5X? (a) SP (b) 16 bit timer (c) XPC (d) 8-bit HPI

10.3 Number of data bus in 54X is ———. (a) 1 (b) 2 (c) 3 (d) 4

10.4 Number of address bus in 54X is ———. (a) 1 (b) 2 (c) 3 (d) 4

10.5 is used to store the result of adder units in the ALU of 54X. (a) Accumlator A (b) Accumlator B (c) Either A or B (d) T Register

10.6 ——— is used to store the result of multiplier units in the ALU of 54X. (a) Accumlator A (b) Accumlator B(c) Either A or B (d) PREG (e) T register

10.7 In the LD || MAC parallel instruction, the register where the MAC result is stored is ———. (a) A (b) B (c) A or B (d) T register

10.8 Bits 32-16 of ——— can be used as an input to the multiplier in 54X. (a) A (b) B (c) Either A or B (d) Neither A or B

10.9 Which of the following registers are present in 5X but not in 54X? (a) PC (b) SP (c) PREG (d) INDX

10.10 The max no. of wait states that software waitstate generator can produce is ———. (a) 1 (b) 4 (c) 7 (d) 8

UNIT-3(MCQ)

1. In general, an FIR system is described by the difference equation y(n)=∑M−1k=0bkx(n−k).  
a) True  
b) False  
View Answer

Answer:a  
Explanation: The difference equation y(n)=∑M−1k=0bkx(n−k) describes the FIR system.

2. What is the general system function of an FIR system?  
a) ∑M−1k=0bkx(n−k)  
b) ∑Mk=0bkz−k  
c) ∑M−1k=0bkz−k  
d) None of the mentioned

Answer:c  
Explanation: We know that the difference equation of an FIR system is given by y(n)=∑M−1k=0bkx(n−k).  
=>h(n)=bk=>∑M−1k=0bkz−k.

3. Which of the following is an method for implementing an FIR system?  
a) Direct form  
b) Cascade form  
c) Lattice structure  
d) All of the mentioned  
View Answer

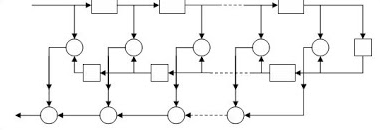
Answer:d  
Explanation: There are several structures for implementing an FIR system, beginning with the simplest structure, called the direct form. There are several other methods like cascade form realization, frequency sampling realization and lattice realization which are used for implementing and FIR system.

4. How many memory locations are used for storage of the output point of a sequence of length M in direct form realization?  
a) M+1  
b) M  
c) M-1  
d) None of the mentioned  
View Answer

Answer:c  
Explanation: The direct form realization follows immediately from the non-recursive difference equation given by y(n)=∑M−1k=0bkx(n−k).  
We observe that this structure requires M-1 memory locations for storing the M-1 previous inputs.

5. The direct form realization is often called a transversal or tapped-delay-line filter.  
a) True  
b) False  
View Answer

Answer:a  
Explanation: The structure of the direct form realization, resembles a tapped delay line or a transversal system.

6. What is the condition of M, if the structure according to the direct form is as follows?  
[](https://www.sanfoundry.com/wp-content/uploads/2015/10/digital-signal-processing-questions-answers-structures-fir-systems-1-q6.png)

a) M even  
b) M odd  
c) All values of M  
d) Doesn’t depend on value of M  
View Answer

Answer:b  
Explanation: When the FIR system has linear phase, the unit sample response of the system satisfies either the symmetry or asymmetry condition, h(n)=±h(M-1-n)  
For such a system the number of multiplications is reduced from M to M/2 for M even and to (M-1)/2 for M odd. Thus for the structure given in the question, M is odd.

7. By combining two pairs of poles to form a fourth order filter section, by what factor we have reduced the number of multiplications?  
a) 25%  
b) 30%  
c) 40%  
d) 50%  
View Answer

Answer:d  
Explanation: We have to do 3 multiplications for every second order equation. So, we have to do 6 multiplications if we combine two second order equations and we have to perform 3 multiplications by directly calculating the fourth order equation. Thus the number of multiplications are reduced by a factor of 50%.

8. The desired frequency response is specified at a set of equally spaced frequencies defined by the equation?  
a) π2M(k+α)  
b) πM(k+α)  
c) 2πM(k+α)  
d) None of the mentioned  
View Answer

Answer:c  
Explanation: To derive the frequency sampling structure, we specify the desired frequency response at a set of equally spaced frequencies, namely ωk=2πM(k+α), k=0,1…(M-1)/2 for M odd  
k=0,1….(M/2)-1 for M even  
α=0 or 0.5.

9. The realization of FIR filter by frequency sampling realization can be viewed as cascade of how many filters?

a) Two  
b) Three  
c) Four  
d) None of the mentioned  
View Answer

Answer:a  
Explanation: In frequency sampling realization, the system function H(z) is characterized by the set of frequency samples {H(k+ α)} instead of {h(n)}. We view this FIR filter realization as a cascade of two filters. One is an all-zero or a comb filter and the other consists of parallel bank of single pole filters with resonant frequencies.

10. What is the system function of all-zero filter or comb filter?  
a) 1M(1+z−Mej2πα)  
b) 1M(1+zMej2πα)  
c) 1M(1−zMej2πα)  
d) 1M(1−z−Mej2πα)  
View Answer

Answer:D  
Explanation: The system function H(z) which is characterized by the set of frequency samples is obtained as  
H(z)=1M(1−z−Mej2πα)∑M−1k=0H(k+α)1−ej2π(k+α)/Mz−1  
We view this FIR realization as a cascade of two filters, H(z)=H1(z).H2(z)  
Here H1(z) represents the all-zero filter or comb filter whose system function is given by the equation  
H1(z)=1M(1−z−Mej2πα).

11. The zeros of the system function of comb filter are located at \_\_\_\_\_\_\_\_\_\_\_\_\_\_  
a) Inside unit circle  
b) On unit circle  
c) Outside unit circle  
d) None of the mentioned  
View Answer

Answer:b  
Explanation: The system function of the comb filter is given by the equation  
H1(z)=1M(1−z−Mej2πα)  
Its zeros are located at equally spaced points on the unit circle at  
zk=ej2π(k+α)/M k=0,1,2….M-1

12. What is the system function of the second filter other than comb filter in the realization of FIR filter?  
a) ∑Mk=0H(k+α)1−ej2π(k+α)Mz−1  
b) ∑M−1k=0H(k+α)1+ej2π(k+α)Mz−1  
c) ∑M−1k=0H(k+α)1−ej2π(k+α)Mz−1  
d) None of the mentioned  
View Answer

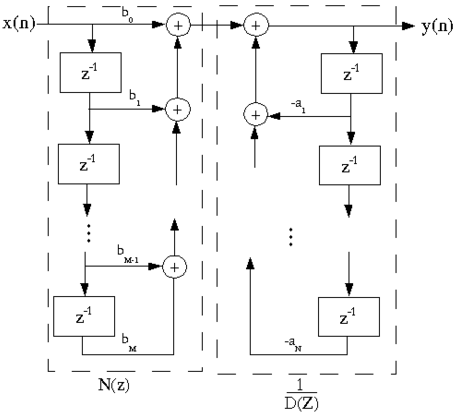
Answer: c  
Explanation: The system function H(z) which is characterized by the set of frequency samples is obtained as  
H(z)=1M(1−z−Mej2πα)∑M−1k=0H(k+α)1−ej2π(k+α)Mz−1  
We view this FIR realization as a cascade of two filters, H(z)=H1(z).H2(z)  
Here H1(z) represents the all-zero filter or comb filter, and the system function of the other filter is given by the equation  
H2(z)=∑M−1k=0H(k+α)1−ej2π(k+α)Mz−1

13. Where does the poles of the system function of the second filter locate?  
a) ej2π(k+α)M  
b) ej2π(k+α)/M  
c) ej2π(k-α)/M  
d) ejπ(k+α)/M  
View Answer

Answer:b  
Explanation: The system function of the second filter in the cascade of an FIR realization by frequency sampling method is given by  
H2(z)=∑M−1k=0H(k+α)1−ej2π(k+α)Mz−1  
We obtain the poles of the above system function by equating the denominator of the above equation to zero.  
=>1−ej2π(k+α)Mz−1=0  
=>z=pk=ej2π(k+α)M, k=0,1….M-1

14. When the desired frequency response characteristic of the FIR filter is narrowband, most of the gain parameters {H(k+α)} are zero.  
a) True  
b) False  
View Answer

Answer:a  
Explanation: When the desired frequency response characteristic of the FIR filter is narrowband, most of the gain parameters {H(k+α)} are zero. Consequently, the corresponding resonant filters can be eliminated and only the filters with nonzero gains need be retained.

15. Which of the following filters have a cascade realization as shown below?  
[](https://www.sanfoundry.com/wp-content/uploads/2015/10/digital-signal-processing-questions-answers-structures-fir-systems-1-q15.png)  
a) IIR filter  
b) Comb filter  
c) High pass filter  
d) FIR filter  
View Answer

Answer:d  
Explanation: The system function of the FIR filter according to the frequency sampling realization is given by the equation  
H(z)=1M(1−z−Mej2πα)∑M−1k=0H(k+α)1−ej2π(k+α)Mz−1  
The above system function can be represented in the cascade form as shown in the above block diagram.